



STIC Search Report

EIC 2100

STIC Database Tracking Number

TO: Cynthia Britt
Location: rnd 2d29
Art Unit : 2133
Monday, May 09, 2005

Case Serial Number: 10/026560

From: Carol Wong
Location: EIC 2100
RND 4A30
Phone: 272-3513

carol.wong@uspto.gov

Search Notes

Dear Examiner Britt,

Attached are the search results (from commercial databases) for your case.

Please call if you have any questions or suggestions for additional terminology, or a different approach to searching the case.

Thanks,
Carol

File 347:JAPIO Nov 1976-2005/Jan(Updated 050506)
(c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200529
(c) 2005 Thomson Derwent
File 344:Chinese Patents Abs Aug 1985-2004/May
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.

Set	Items	Description
S1	2403173	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	692571	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS OR CHIP? ? OR MICROCHIP? ?
S3	670600	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	848004	TEST OR TESTER? OR TESTED OR TESTING OR TESTS OR SELFTEST? OR BIST OR EVALUAT?
S5	132835	S4(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S6	39316	S4(3N)S1:S2
S7	878833	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	92177	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	638179	READ OR READS OR READING
S10	11293	S9(5N) (ANOTHER OR OTHER)
S11	95720	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR THIRDS OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWEEN)
S12	23637	S9(5N) (NUMBER OR PAIR?? ?)
S13	1797	S7(5N)S8
S14	257	S7(5N)S10
S15	2550	S7(5N)S11:S12
S16	29	(S5:S6 OR S3) AND S13 AND S14:S15
S17	29	IDPAT (sorted in duplicate/non-duplicate order)
S18	29	IDPAT (primary/non-duplicate records only)
S19	22637	IC='G11C-029/00':IC='G11C-029/04'
S20	38159	IC='G01R-031/28':IC='G01R-031/288'
S21	7587	MC=S01-G02B
S22	4874	MC=T01-J07B1
S23	3426	MC=U11-F01C5
S24	400	MC=U14-D09
S25	30	S19:S24 AND S13 AND S14:S15
S26	14	S25 NOT S18
?		

18/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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016021440 **Image available**
WPI Acc No: 2004-179291/200417
Related WPI Acc No: 2004-633581
XRPX Acc No: N04-142586

Semiconductor memory fault testing method e.g. for dynamic random access memory, involves comparing bits read from different memory blocks with each other, to determine fault

Patent Assignee: BAUM A M (BAUM-I); CALLAWAY B P (CALL-I); MICRON TECHNOLOGY INC (MICR-N)

Inventor: BAUM A M; CALLAWAY B P

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040015754	A1	20040122	US 2002199151	A	20020718	200417 B
US 6879530	B2	20050412	US 2002199151	A	20020718	200525

Priority Applications (No Type Date): US 2002199151 A 20020718

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040015754	A1		15	G11C-007/00	
US 6879530	B2			G11C-007/00	

Abstract (Basic): US 20040015754 A1

NOVELTY - The specific pattern of bits written in each memory block comprising several memory bits, are read from respective memory blocks and compared with each other. When the read bits of one memory block differs from read bits of another memory block, it is determined that fault is occurred in the memory block.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (1) semiconductor memory;
- (2) circuit for repairing memory with faulty memory block;
- (3) method for dynamically testing and repairing memory; and
- (4) electronic system.

USE - For testing occurrence of faults in semiconductor memory (claimed) such as dynamic random access memory (DRAM), static random access memory (SRAM) used in electronic system (claimed).

ADVANTAGE - By comparing the bits of the memory block with each other, the faults are detected accurately, thereby eliminating the problem of not detecting similar localized faults in adjacent blocks of memory.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the exemplary memory.

memory (40)
memory address and control bus (42)
input data bus (44)
output data bus (46)
internal control bus (48)
pp; 15 DwgNo 1/9

Title Terms: SEMICONDUCTOR; MEMORY; FAULT; TEST; METHOD; DYNAMIC; RANDOM;

ACCESS; MEMORY; COMPARE; BIT; READ; MEMORY; BLOCK; DETERMINE; FAULT

Derwent Class: S01; U14; U21

International Patent Class (Main): G11C-007/00

International Patent Class (Additional): G11C-029/00

File Segment: EPI

Manual Codes (EPI/S-X): S01-G01A; U14-A03B; U14-D01A; U14-D01B; U21-C03D1

18/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

015250413 **Image available**
WPI Acc No: 2003-311339/200330
XRPX Acc No: N03-247801

Memory circuit testing method e.g. in semiconductor device,
involves selecting memory circuits and comparing read data with one
another and with write data

Patent Assignee: FUJITSU LTD (FUJIT); FUJITSU VLSI LTD (FUIV)

Inventor: HIBINO S; TAKESHIGE M; YAMADA K

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020188900	A1	20021212	US 200126560	A	20011227	200330 B
KR 2002095028	A	20021220	KR 20022029	A	20020114	200330
JP 2002365338	A	20021218	JP 2001174101	A	20010608	200330

Priority Applications (No Type Date): JP 2001174101 A 20010608

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020188900	A1		18	G11C-029/00	
KR 2002095028	A			G11C-029/00	
JP 2002365338	A		12	G01R-031/28	

Abstract (Basic): US 20020188900 A1

NOVELTY - Several memory circuits (RAM0-RAM3) are simultaneously selected, and the read / write operation of the memory circuits is performed. The data read from the memory circuits are compared with one another, and one of the read data is also compared with the write data, during the test mode.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) semiconductor device; and
- (2) memory circuit testing system.

USE - For testing random access memory (RAM) circuits in semiconductor device (claimed) such as large scale integrated (LSI) circuit.

ADVANTAGE - Shortens the memory circuit testing time and cost, since the time needed to access the memory circuits becomes shorter by simultaneous selection of the memory circuits.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic block diagram of the semiconductor device.

memory circuits (RAM0-RAM3)

pp; 18 DwgNo 1/15

Title Terms: MEMORY; CIRCUIT; TEST; METHOD; SEMICONDUCTOR; DEVICE; SELECT;
MEMORY; CIRCUIT; COMPARE; READ; DATA; ONE; WRITING; DATA

Derwent Class: S01; T01; U11; U14

International Patent Class (Main): G01R-031/28; G11C-029/00

File Segment: EPI

Manual Codes (EPI/S-X): S01-G02B; T01-J07B1; U11-F01C5; U14-D09

18/9/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

014465182 **Image available**

WPI Acc No: 2002-285885/200233

XRPX Acc No: N02-223568

Quality judging board for burn-in test system, outputs trigger to write
quality judging result in memory when data arbitrarily designated to
tested device and corresponds with predetermined reference value

Patent Assignee: ANDO ELECTRIC CO LTD (ANDN)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001324547	A	20011122	JP 2000145319	A	20000517	200233 B

Priority Applications (No Type Date): JP 2000145319 A 20000517

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001324547	A		6 G01R-031/28	

Abstract (Basic): JP 2001324547 A

NOVELTY - The judging board (10) has a judgment unit (2), which
judges the quality of burn-in test result based on output of a
comparator (1) which compares burn-in test result output from a tested
device (20), with predetermined comparison value. Another
comparator (5) outputs trigger to reading / writing controlled
circuit (6) for writing quality judging result in a memory (4), when
data arbitrarily designated to device corresponds with predetermined
reference value.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
burn-in test quality judging result storing method.

USE - For testing function and electrical properties of integrated
circuit.

ADVANTAGE - Enables real time quality judging of several judgment
boards. Quality judging result can be written in memory at arbitrary
timing for each quality judging board.

DESCRIPTION OF DRAWING(S) - The figure shows the circuit component
of judgment board of burn-in test system. (Drawing includes non-English
language text).

Comparators (1,5)

Judgment unit (2)

Memory (4)

Reading/writing controlled circuit (6)

Judging board (20)

Tested device (20)

pp; 6 DwgNo 1/2

Title Terms: QUALITY; JUDGEMENT; BOARD; BURN; TEST; SYSTEM; OUTPUT; TRIGGER
; WRITING; QUALITY; JUDGEMENT; RESULT; MEMORY; DATA; ARBITRARY;

DESIGNATED; TEST; DEVICE; CORRESPOND; PREDETERMINED; REFERENCE; VALUE

Derwent Class: S01; U11

International Patent Class (Main): G01R-031/28

International Patent Class (Additional): G01R-031/30; G11C-029/00;

H01L-021/66

File Segment: EPI

Manual Codes (EPI/S-X): S01-G01A1; S01-G01A5; U11-F01C3; U11-F01D2;

U11-F01G

? t18/9/15

18/9/15 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009041238 **Image available**

WPI Acc No: 1992-168597/199221

XRPX Acc No: N92-127076

Fault analysis of memory incorporating redundancy circuit - uses fault address memory with cells corresponding, by predetermined rule, and to several cells of memory under test

Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA CORP (TOKE)

Inventor: TSUKAKOSHI H

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 485976	A2	19920520	EP 91119337	A	19911113	199221 B
EP 485976	A3	19930414	EP 91119337	A	19911113	199351
US 5363382	A	19941108	US 91791171	A	19911113	199444
EP 485976	B1	19970604	EP 91119337	A	19911113	199727
DE 69126400	E	19970710	DE 626400	A	19911113	199733
			EP 91119337	A	19911113	
KR 9513401	B1	19951108	KR 9120081	A	19911112	199901

Priority Applications (No Type Date): JP 90306452 A 19901113

Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 125633; GB 2206715; US 4627053

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 485976	A2	E 10	G11C-029/00	
			Designated States (Regional): DE FR GB	
US 5363382	A	9	G01R-031/28	
EP 485976	B1	E 12	G11C-029/00	
			Designated States (Regional): DE FR GB	
DE 69126400	E		G11C-029/00	Based on patent EP 485976
EP 485976	A3		G11C-029/00	
KR 9513401	B1		G11C-029/00	

Abstract (Basic): EP 485976 A

A memory (50) which incorporates a redundancy circuit is tested for faults using an algorithmic pattern generator (2). The data written into and read from a memory cell is compared (4). Disagreement causes ONE to be written into an appropriate cell of a fault analysis memory (8).

Each cell of the latter corresponds, by a predetermined rule, employed by an address allocation circuit (6), to a plurality of cells of the memory under test. Thereafter, it is judged if a disclosed fault can be remedied using the redundancy circuit.

ADVANTAGE - Reduced space and judgement time.

Dwg.3/9

Abstract (Equivalent): EP 485976 B

An apparatus for analyzing faults in a memory having a redundancy circuit, comprising: an algorithmic pattern generator (2) for generating address signals that select a memory cell of a memory under test (50) having a redundancy circuit and for generating data that is written to a selected memory cell of the memory under test (50); comparison means (4) for performing a data read operation one selected cell of the memory under test (50) after data has been written to a memory cell selected by said address signals and then for comparing said read data and said data from said algorithmic pattern generator (2) for whether or not it is in agreement and if it is not in agreement generates a fault signal that indicates that the memory cell is faulty; and a fault analysis memory (8) having a plural number of memory cells; and said apparatus for analyzing faults being characterized by further comprising: address allocation means (6) for receiving address signals from said algorithmic pattern generator (2) and performing address allocation for said fault analysis memory (8) so

that a block of a plurality number of memory cells of said **memory** under **test** (50) corresponds to the basis of a predetermined rule to a single memory cell of said fault analysis memory (8), the dimensions of one block being at least two cells in the column direction and at least two cells in the row direction; and means for writing a fault information in a single memory cell of said fault analysis memory (8) if a fault signal has been generated for at least one of said corresponding plural number of memory cells.

Dwg.3/9

Abstract (Equivalent): US 5363382 A

The appts includes an algorithmic pattern generator for generating address signals to select memory cells in a **memory** under **test** (MUT). The **MUT** is a measurement object having a redundancy circuit, while the algorithmic pattern generator generating data supplied to the selected memory cells.

The appts also incorporates a **comparison** device for performing a **read** operation of the data after data have been **written** into the selected memory cells selected by the address signals and comparing data read with the data supplied from the algorithmic pattern generator to determine whether or not both the data read and the data from the algorithmic pattern generator are in agreement.

USE/ADVANTAGE - For individual fault **test** analysis for **memory** cells with redundancy circuits. Reduced capacity of fault analysis memory, and reducing time for judging whether or not recovery is possible.

Dwg.3/9

Title Terms: FAULT; ANALYSE; MEMORY; INCORPORATE; REDUNDANT; CIRCUIT; FAULT ; ADDRESS; MEMORY; CELL; CORRESPOND; PREDETERMINED; RULE; CELL; MEMORY; TEST

Derwent Class: T01; U14

International Patent Class (Main): G01R-031/28; G11C-029/00

International Patent Class (Additional): G06F-011/20

File Segment: EPI

Manual Codes (EPI/S-X): T01-G03; T01-H01C4; U14-D01; U14-D03

? t18/9/24,27

18/9/24 (Item 24 from file: 347)

DIALOG(R)File 347:JAPIO

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02887100 **Image available**

MEMORY TEST EQUIPMENT

PUB. NO.: 01-184700 [JP 1184700 A]

PUBLISHED: July 24, 1989 (19890724)

INVENTOR(s): FUJISAKI KENICHI

APPLICANT(s): ADVANTEST CORP [359339] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 63-004181 [JP 884181]

FILED: January 11, 1988 (19880111)

INTL CLASS: [4] G11C-029/00

JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 46.2 (INSTRUMENTATION -- Testing)

JOURNAL: Section: P, Section No. 949, Vol. 13, No.. 471, Pg. 33, October 25, 1989 (19891025)

ABSTRACT

PURPOSE: To obtain an image **memory** **test** equipment of simple constitution by providing a **memory** to be **tested**, a buffer **memory**, a data register, a multiplexer, a mask data register, and a mask control

part.

CONSTITUTION: A memory 200 to be tested is switched to a flash mode by the signal of a control signal generating part 109. When the memory 200 executes flash write, a buffer memory 400 is set to the write state and writes data of a data register 501 in an address area in the same row as write in the memory 200 in accordance with the address signal of a pattern generator 100. In this case, a mask control part 600 writes data after masking it with data of a mask register 601 or OR between this data and input mask data from the pattern generator 100. The memory 200 and the buffer memory 400 are switched to the read state at the time of completing the write in the buffer memory 400, and read outputs are compared with each other by a logical comparator 300 to decide whether the memory to be tested is good or not.

18/9/27 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO
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01866243 **Image available**
TESTING METHOD OF MOUNTED MEMORY

PUB. NO.: 61-080343 [JP 61080343 A]
PUBLISHED: April 23, 1986 (19860423)
INVENTOR(s): YAZAKI TOSHIYUKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-202210 [JP 84202210]
FILED: September 27, 1984 (19840927)
INTL CLASS: [4] G06F-012/16; G06F-001/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.9
(INFORMATION PROCESSING -- Other)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 492, Vol. 10, No. 254, Pg. 48, August
30, 1986 (19860830)

ABSTRACT

PURPOSE: To shorten a testing time by forming a table for making coordinates indicating the position of a memory element correspond to its address and analyzing an error bit on the basis of an error generation address and reading/ writing data to specify and display the error generating memory element.

CONSTITUTION: When a memory printing plate 21 to be tested which is a main memory part is to be tested by a control part 20, a table for making the coordinates indicating the position of a memory element on the plate 21 correspond to a memory element accessing address is stored in a floppy disc 23. Writing data is written on the memory to be tested to read out its contents and both the writing and reading data are compared with each other. If both the data are dissident, the table of the corresponding address is extracted and stored in a storage part 22. Then, a dissident bit is detected, a flag is set in the corresponding bit of the table, the table of the error generation address is displayed, and the position of the flag is blinked.

File 348:EUROPEAN PATENTS 1978-2005/May W01
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050505,UT=20050428
(c) 2005 WIPO/Univentio
File 324:German Patents Fulltext 1967-200517
(c) 2005 Univention

Set	Items	Description
S1	872294	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	424730	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS OR CHIP? ? OR MICROCHIP? ?
S3	990430	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	947095	TEST OR TESTER? OR TESTED OR TESTING OR TESTS OR SELFTEST? OR BIST OR EVALUAT?
S5	118331	S4(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S6	23202	S4(3N)S1:S2
S7	1233790	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	78847	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	537904	READ OR READS OR READING
S10	44450	S9(5N) (ANOTHER OR OTHER)
S11	118502	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR THIRDS OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWEEN)
S12	27307	S9(5N) (NUMBER OR PAIR?? ?)
S13	2106	S7(5N)S8
S14	488	S7(5N)S10
S15	3389	S7(5N)S11:S12
S16	108	(S5:S6 OR S3) (20N)S13
S17	15	S16(20N)S14:S15
S18	15	IDPAT (sorted in duplicate/non-duplicate order)
S19	14	IDPAT (primary/non-duplicate records only)
S20	2713	IC='G11C-029'
S21	4199	IC='G01R-031/28'
S22	6756	S20:S21
S23	21	S22 AND S13(20N)S14:S15
S24	11	S23 NOT S17
S25	11	IDPAT (sorted in duplicate/non-duplicate order)
S26	11	IDPAT (primary/non-duplicate records only)

File 348:EUROPEAN PATENTS 1978-2005/May W01
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050505,UT=20050428
(c) 2005 WIPO/Univentio
File 324:German Patents Fulltext 1967-200517
(c) 2005 Univentio

Set	Items	Description
S1	872294	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT- OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	272510	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS
S3	990430	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	749064	TEST OR TESTER? OR TESTED OR TESTING OR TESTS
S5	70796	S4(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MO- DULE? OR UNIT OR UNITS)
S6	23580	S4(3N)S1:S3
S7	1233790	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	78847	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	537904	READ OR READS OR READING
S10	44450	S9(5N) (ANOTHER OR OTHER)
S11	118502	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR T- HIRD OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWE- EN)
S12	27307	S9(5N) (NUMBER OR PAIR?? ?)
S13	2106	S7(5N)S8
S14	488	S7(5N)S10
S15	3389	S7(5N)S11:S12
S16	93	S5:S6(20N)S13
S17	15	S16(20N)S14:S15
S18	15	IDPAT (sorted in duplicate/non-duplicate order)
S19	14	IDPAT (primary/non-duplicate records only)
S20	205141	CHIP? ? OR MICROCHIP? ?
S21	4690	S4(3N)S20
S22	7417	(SELFTEST? OR BIST OR EVALUAT?) (3N) (S1:S3 OR S20)
S23	52610	(SELFTEST? OR BIST OR EVALUAT?) (3N) (DEVICE? ? OR CIRCUIT? - OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S24	16	S21:S23(20N)S13
S25	1	S24(20N)S14:S15

? t19/5,k/11

19/5,K/11 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00546715 **Image available**

A SYSTEM, METHOD, AND PROGRAM FOR DETECTING AND ASSURING DRAM ARRAYS
SYSTEME, PROCEDE ET PROGRAMME PERMETTANT DE DETECTER DES MATRICES A MEMOIRE
RAM DYNAMIQUE ET A EN ASSURER L'INTEGRITE

Patent Applicant/Assignee:

ERICSSON INC,

Inventor(s):

MORRIS Joseph Norman,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200010088 A1 20000224 (WO 0010088)

Application: WO 99US16843 19990723 (PCT/WO US9916843)

Priority Application: US 98131814 19980810

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE
GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN
MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA
ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY
DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML
MR NE SN TD TG

Main International Patent Class: G06F-011/22

International Patent Class: G11C-029/00

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 6477

English Abstract

A system, method, and program for detecting and assuring a row by column structure in a Dynamic Random Access Memory array is disclosed. By writing to and reading from each memory location of the DRAM array, memory integrity is assured. The number of columns in the DRAM array is identified by writing data to and reading data from addresses selected from a series of cell addresses. The series of cell addresses identify standard DRAM column structures. When the data written to and read from the cell address is identical, the column configuration of the DRAM arrays is identified. The number of rows in the memory array is then identified by writing data to and reading data from addresses selected from a second series of cell addresses. The second series of cell addresses identify standard DRAM row structures. When data written to and read from the cell address is identical, the row configuration of the DRAM array is identified and accordingly, the row by column structure and integrity of the DRAM array are known.

French Abstract

La presente invention concerne un systeme, un procede et un programme qui permettent de detecter une structure en rangees/colonnes de matrice RAM dynamique (DRAM) et a en assurer l'integrite. Le fait d'ecrire et de lire a chaque emplacement de memoire de la matrice RAM dynamique permet d'assurer l'integrite de la memoire. Pour identifier le nombre de colonnes de la matrice RAM dynamique, on ecrit et on lit des donnees a partir d'adresses prises dans une serie d'adresses cellules. Cette serie d'adresses cellules permet d'identifier des structures en colonne DRAM

standard. Lorsque les donnees ecrites et lues dans l'adresse cellule sont identiques, il est possible d'identifier la configuration en colonnes des matrices DRAM. Pour determiner le nombre de rangees dans la matrice de memoire, on ecrit et on lit ensuite des donnees dans des adresses prises dans une secondes serie d'adresses de cellules. Cette seconde serie d'adresses de cellules permet d'identifier des structures en rangee DRAM standard. Lorsque les donnees lues et ecrites dans l'adresse de cellule sont identiques, on peut identifier la configuration en rangee de la memoire RAM dynamique et, par la meme, connaitre la rangee de la structure en colonne et assurer l'integrite de la memoire DRAM.

Fulltext Availability:

Claims

Claim

... address corresponding to the maximum row boundary address less the row-modifier; and then,
(1) **testing** the second **memory** address by writing data to and **reading** data from the **second** memory address; and then, **comparing** the data **read** from the **second** memory address to the data **written** to the second memory address; and then,
(k) calculating the row-modifier, and then,
(1...

? t19/5, k/13-14

19/5, K/13 (Item 13 from file: 324)

DIALOG(R) File 324: German Patents Fulltext

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0004035346 **Image available**

Memory module with a test equipment

Speichermodul mit einer Testeinrichtung

Patent Applicant/Assignee:

Infineon Technologies AG, 81669 Munchen, DE

Inventor(s):

Jakobs Andreas, Dr., 81673 Munchen, DE

Patent and Priority Information (Country, Number, Date):

Patent: DE 10260184 A1 20040715

Application: DE 10260184 20021220

Priority Application: DE 10260184 20021220 (DE 10260184)

Main International Patent Class: G11C-029/00

Publication Language: German

Fulltext Availability:

Description (English machine translation)

Claims (English machine translation)

Description (German)

Claims (German)

Fulltext Word Count (English): 3375

Fulltext Word Count (German) : 2663

Fulltext Word Count (Both) : 6038

Abstract (English machine translation)

A memory module (9) is described, an module-internal, component-spreading electrical function test of several integrated memory modules (1, 2, 3, 4), which on a printed circuit board (7) the memory module (9) is arranged, made possible. For this according to invention a test equipment (5) is intended, which is separately by the memory modules (1, 2, 3, 4) on the printed circuit board arranged. The test equipment (5) is dependent on a clock pulse made available by an external test equipment (10) (T) and cannot indicate a test result, produced however the test signal on necessary for the execution of the function test and passes this over control lines (11), address lines (12), data lines (14)

as well as lines (13) for selecting individual memory modules (1, 2, 3, 4) to these. The partial integration of test functions into the test equipment according to invention (5) makes a larger independence possible in relation to outside electromagnetic influences of noise without all too large increase of the space requirement of the memory module.

Abstract (German)

Es wird ein Speichermodul (9) beschrieben, das einen modulinternen, bausteinübergreifenden elektrischen Funktionstest mehrerer integrierter Speicherbausteine (1, 2, 3, 4), die auf einer Leiterplatte (7) des Speichermoduls (9) angeordnet sind, ermöglicht. Hierzu ist erfindungsgemäss eine Testeinrichtung (5) vorgesehen, die separat von den Speicherbausteinen (1, 2, 3, 4) auf der Leiterplatte angeordnet ist. Die Testeinrichtung (5) ist auf ein von einem externen Testgerät (10) bereitgestelltes Taktsignal (T) angewiesen und kann ein Testergebnis nicht selbst anzeigen, erzeugt jedoch die für die Durchführung des Funktionstests erforderlichen Testsignale und leitet diese über Steuerleitungen (11), Adressleitungen (12), Datenleitungen (14) sowie Leitungen (13) zum Auswählen einzelner Speicherbausteine (1, 2, 3, 4) an diese weiter. Die teilweise Integration von Testfunktionen in die erfindungsgemässe Testeinrichtung (5) ermöglicht eine grossere Unabhängigkeit gegenüber äusseren elektromagnetischen Storeinflüssen ohne allzu grosse Erhöhung des Platzbedarfs des Speichermoduls.

Fulltext Availability:

Description (English machine translation)

Description (English machine translation)

... test in order to already guarantee before the assembly an error free enterprise of the memory module . With the function test , which is accomplished memory module-internally in each case, information in storage addresses is written and selected from them, whereby written and read information is compared with one another . A further function test, which essentially functions according to the same principle, is accomplished after...

19/5,K/14 (Item 14 from file: 324)

DIALOG(R)File 324:German Patents Fulltext

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0004003921 **Image available**

Permanent chip ID using a FeRAM

Permanente Chip-ID unter Verwendung eines FeRAM

Patent Applicant/Assignee:

Agilent Technologies Inc (an d Ges d Staates Delaware), Palo Alto, Calif.,
US

Inventor(s):

McAdams Hugh P, Texas, US

Grace James W, Los Altos Hills, Calif., US

Patent and Priority Information (Country, Number, Date):

Patent: DE 10318183 A1 20040129

Application: DE 10318183 20030422

Priority Application: US 2002190408 20020702 (US 19040802)

Main International Patent Class: G11C-029/00

International Patent Class: G11C-011/22

Publication Language: German

Fulltext Availability:

Description (English machine translation)

Claims (English machine translation)

Description (German)

Claims (German)
Fulltext Word Count (English): 3511
Fulltext Word Count (German) : 3198
Fulltext Word Count (Both) : 6709

Abstract (English machine translation)

A IC chip contains a small non volatile "ID" memory, e.g. an FeRAM array, which stores information, those the production, testing and the behavior of the IC chip are assigned to which. The stored information can cover a seriennummer, a wafer ID, a lot ID, a datencode, a chip history, test datas and behavior information, is not limited however not to the same. Storing information on the chip eliminates arbitrary difficulties with the adaptation of the information to the IC chip and supplies a flexible permanent recording of arbitrary information, which useful the manufacturer may find. The ID memory permits thus a pursuing and an identification from ICs to a degree, which was so far not practicable.

Abstract (German)

Ein IC-Chip enthält einen kleinen nichtfluchtigen "ID"-Speicher, wie z. B. ein FeRAM-Array, das Informationen speichert, die der Herstellung, dem Testen und dem Verhalten des IC-Chips zugeordnet sind. Die gespeicherten Informationen können eine Seriennummer, eine Wafer-ID, eine Los-ID, einen Datencode, eine Chiphistorie, Testdaten und Verhaltensinformationen umfassen, sind jedoch nicht auf dieselben beschränkt. Das Speichern von Informationen auf dem Chip beseitigt beliebige Schwierigkeiten beim Anpassen der Informationen an den IC-Chip und liefert eine flexible permanente Aufzeichnung von beliebigen Informationen, die der Hersteller nützlich finden mag. Der ID-Speicher erlaubt somit ein Verfolgen und eine Identifizierung von ICs bis zu einem Grad, der bisher nicht praktikierbar war.

Fulltext Availability:

Description (English machine translation)

Description (English machine translation)

... to compare or refurbish around the test results, which were not stored in the ID memory, the stored test results with other stored test results. Additional test -, writing results, read results and results of comparison can be implemented before and/or after the Haeusen of the IC chip, to is...

?

26/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01147948

Method of testing random-access memory

Prüfungsverfahren eines dynamischen Speichers

Procede de test d'une memoire d'access aleatoire

PATENT ASSIGNEE:

LUCENT TECHNOLOGIES INC., (2143720), 600 Mountain Avenue, Murray Hill,
New Jersey 07974-0636, (US), (Applicant designated States: all)

INVENTOR:

Kroon, Adriaan, Ouderhoek 70, 3632 XG Loenen aan der Vecht, (NL)

LEGAL REPRESENTATIVE:

Williams, David John et al (86433), Page White & Farrer, 54 Doughty
Street, London WC1N 2LS, (GB)

PATENT (CC, No, Kind, Date): EP 1001432 A1 000517 (Basic)

APPLICATION (CC, No, Date): EP 98309192 981110;

DESIGNATED STATES: DE; FR; GB; NL

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G11C-029/00

ABSTRACT EP 1001432 A1

A method of testing RAM without destroying the stored data consists of looping through the locations to be tested (21, 28, 29), and at each location, inverting the data stored in the location (22), loading the inverted data from the location to a register (23), inverting the data in the register (24), writing the twice-inverted data back to the location (25) and comparing the actual content of the location with the content of the register (26). The test fails (27) if any of the comparisons fails, whereupon the test can be terminated. The test succeeds (30) if the all of the locations have been tested without any of the comparisons having failed. Further tests may be carried out at a selected location only, to test for short circuits between data bus leads. The method contains fewer memory access operations than the conventional method, so it will be faster. The method will also detect bits that can be changed but not changed back again, as well as stuck bits.

ABSTRACT WORD COUNT: 169

NOTE:

Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 000517 A1 Published application with search report

Examination: 010103 A1 Date of request for examination: 20001106

Change: 010516 A1 Legal representative(s) changed 20010329

Withdrawal: 031203 A1 Date application deemed withdrawn: 20030531

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200020	342
SPEC A	(English)	200020	1571
Total word count - document A			1913
Total word count - document B			0
Total word count - documents A + B			1913

INTERNATIONAL PATENT CLASS: G11C-029/00

...SPECIFICATION comparison will fail unless both changes are correctly made. Furthermore, the method contains only two **write** operations in addition to **three read** operations and only has one **comparison**

instruction and one conditional jump.

Brief Description of the Drawings

An embodiment of the invention...
? t26/5,k/7

26/5,K/7 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00549813 **Image available**

METHOD AND SYSTEM FOR TIMING CONTROL IN THE TESTING OF RAMBUS MEMORY
MODULES

PROCEDE ET SYSTEME POUR COMMANDER LA TEMPORISATION LORS DE TESTS DE MODULES
DE MEMOIRE RAMBUS

Patent Applicant/Assignee:

TANISYS TECHNOLOGY INC,

Inventor(s):

HUNTER Paul R,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200013186 A1 20000309 (WO 0013186)

Application: WO 99US19752 19990825 (PCT/WO US9919752)

Priority Application: US 9897894 19980826; US 99267731 19990315; US
99359173 19990722

Designated States:

(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)

AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK EE ES FI GB GD
GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG
MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN
YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE
CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN
GW ML MR NE SN TD TG.

Main International Patent Class: G11C-029/00

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 9620

English Abstract

A system and method for testing a RIMM loaded with RDRAM integrated circuits generates and reads test transaction data with a test transaction engine, such as a microprocessor-based memory tester. A RIMM adapter interfaces with the test transaction engine and the RIMM under test to communicate test data, including test write, address, control and read data. A comparison of test read data returned to the test transaction engine from the RIMM against predetermined values allows a determination of the operational status of the RIMM. A load circuit skews the clock timing signal by a programmable amount relative to a constant data signal to allow testing of setup and hold time, and simulation of various trace length conditions. The RIMM adapter is embodied as an ASIC with plural FIFO circuits interfaced between the test transaction engine and a channel controller and RAC. The FIFOs reconcile differences in timing between generation and return of test data and demands by the RAC and channel controller. Separate read and write data paths between the test transaction engine and ASIC support improved rates of data transfer. The test transaction engine provides full speed test transactions by using instruction data to generate test data with FPGAs.

French Abstract

Selon cette invention, un systeme et un procede pour tester un module RIMM charge de circuits integres de memoires RDRAM servent a generer et a lire des donnees de transaction test avec un moteur de transactions tel qu'un testeur de memoire base sur des microprocesseurs. Un adaptateur de RIMM assure l'interface avec un moteur de transactions de test et le module RIMM teste pour communiquer les donnees de test, y compris les donnees d'ecriture, d'adresse, de commande et de lecture de test. Une comparaison de donnees de lecture de test, retournee au moteur de transactions de test depuis le module RIMM contre des valeurs predeterminees, permet de determiner le statut de fonctionnement du module RIMM. Un circuit de charge decale un signal d'horloge de temporisation pour une valeur programmable relative a un signal constant de donnees afin de permettre la verification du temps de mise en place et de prise ainsi que la simulation de divers etats de longueur de traces. L'adaptateur de RIMM est realise sous la forme d'un circuit integre specifique (ASIC) comportant plusieurs circuits FIFO connectes entre le moteur de transactions de test, un controleur de canal et une cellule de voies ASIC de RAMBUS (RAC). Les circuits FIFO egalisent les differences de temporisation entre la generation et le retour de donnees test et les demandes par le RAC et le controleur de canal. Les chemins separes de lecture et d'ecriture de donnees entre le moteur de transactions de test et le support d'ASIC permettent d'ameliorer les debits de transmission de donnees. Le moteur de transactions de test assure des transactions de donnees a toute vitesse en utilisant des donnees d'instructions pour generer des tests de donnees avec des prediffuses programmables.

Main International Patent Class: G11C-029/00

Fulltext Availability:

Detailed Description

Detailed Description

... from a

RIMM. Mask circuit 118, compare circuit 120 and error circuit 122 provide a **comparison between test write data** and test **read** data to detect differences that indicate an error with the RIMM that provided the test...

?

File 6:NTIS 1964-2005/May W1
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File 2:INSPEC 1969-2005/Apr W4
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File 8:EI Compendex(R) 1970-2005/May W1
(c) 2005 Elsevier Eng. Info. Inc.
File 34:SciSearch(R) Cited Ref Sci 1990-2005/May W1
(c) 2005 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2005/Apr
(c) 2005 ProQuest Info&Learning
File 65:Inside Conferences 1993-2005/May W2
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File 94:JICST-EPlus 1985-2005/Mar W3
(c) 2005 Japan Science and Tech Corp(JST)
File 99:Wilson Appl. Sci & Tech Abs 1983-2005/Apr
(c) 2005 The HW Wilson Co.
File 144:Pascal 1973-2005/May W1
(c) 2005 INIST/CNRS
File 256:TecInfoSource 82-2005/Mar
(c) 2005 Info.Sources Inc
File 266:FEDRIP 2005/Jan
Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
(c) 2002 The Gale Group

Set	Items	Description
S1	2471069	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	787757	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS OR CHIP? ? OR MICROCHIP? ?
S3	373150	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	9015042	TEST OR TESTER? OR TESTED OR TESTING OR TESTS OR SELFTEST? OR BIST OR EVALUAT?
S5	252149	S4(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S6	73734	S4(3N)S1:S2
S7	6851396	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	33813	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	289824	READ OR READS OR READING
S10	5245	S9(5N) (ANOTHER OR OTHER)
S11	39822	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR THIRD OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWEEN)
S12	4441	S9(5N) (NUMBER OR PAIR?? ?)
S13	470	S7(5N)S8
S14	139	S7(5N)S10
S15	1260	S7(5N)S11:S12
S16	7	(S5:S6 OR S3) AND S13 AND S14:S15
S17	7	S16/2001:2005
S18	0	S16 NOT S17
S19	68	S13 AND S14:S15
S20	25	S19 AND S1:S3
S21	19	S19 AND (RAM OR RAMS OR STORAGE OR RAS OR DRAM? ? OR SRAM? ? OR SDRAM? OR RDRAM? OR SLDRAM? OR DDR? ? OR SGRAM? OR DRDRAM? OR DDRAM?)
S22	29	S20:S21
S23	24	S22/2002:2005
S24	5	S22 NOT S23

S25	7	S16/2002:2005
S26	0	S16 NOT S25
S27	4	RD S24 (unique items)
?		

27/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7138023 INSPEC Abstract Number: C2002-02-5130-008

Title: Automatic abstraction of memories in the formal verification of superscalar microprocessors

Author(s): Velez, M.N.

Author Affiliation: Dept. of Electr. & Comput. Eng., Carnegie Mellon Univ., Pittsburgh, PA, USA

Conference Title: Tools and Algorithms for the Construction and Analysis of Systems. 7th International Conference, TACAS 2001. Held as Part of the Joint European Conferences on Theory and Practice of Software, ETAPS 2001. Proceedings (Lecture Notes in Computer Science Vol.2031) p.252-67

Editor(s): Margaria, T.; Yi, W.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 2001 Country of Publication: Germany xiv+588 pp.

ISBN: 3 540 41865 2 Material Identity Number: XX-2001-01784

Conference Title: Tools and Algorithms for the Construction and Analysis of Systems

Conference Date: 2-6 April 2001 Conference Location: Genova, Italy

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: A system of conservative transformation rules is presented for abstracting **memories** whose forwarding logic interacts with stalling conditions for preserving the **memory** semantics in microprocessors with in-order execution. Microprocessor correctness is expressed in the logic of equality with uninterpreted functions and **memories** (EUFM). **Memory** reads and writes are abstracted as arbitrary uninterpreted functions in such a way that the forwarding property of the **memory** semantics-that a read returns the data most recently written to an equal write address-is satisfied completely only when exactly the same **pair** of one **read** and one **write** address is **compared** for equality in the stalling logic. These transformations are applied entirely automatically by a tool for formal verification of microprocessors, based on EUFM, the Burch and Dill (1994) flushing technique, and the properties of positive equality. An order of magnitude reduction is achieved in the number of e/sub ij/ Boolean variables that encode the equality comparisons of register identifiers in the correctness formulas for single-issue pipelined and dual-issue superscalar microprocessors with multicycle functional units, exceptions, and branch prediction. That results in up to 40* reduction in the CPU time for the formal verification of the dual-issue superscalar microprocessors.

(22 Refs)

Subfile: C

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27/7/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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6198654 INSPEC Abstract Number: B1999-05-3120B-050

Title: Carrier erasure current method for in-situ monitoring of head-disk spacing variation.

Author(s): Bo Liu; Qisuo Chen

Author Affiliation: Data Storage Inst., Singapore

Journal: IEEE Transactions on Magnetics Conference Title: IEEE Trans. Magn. (USA) vol.35, no.2, pt.1 p.939-44

Publisher: IEEE,

Publication Date: March 1999 Country of Publication: USA

CODEN: IEMGAQ ISSN: 0018-9464
SICI: 0018-9464(199903)35:2:1L.939:CECM;1-T
Material Identity Number: I101-1999-004
U.S. Copyright Clearance Center Code: 0018-9464/99/\$10.00
Conference Title: Second Asia-Pacific Magnetic Recording Conference (APMRC'98)

Conference Date: 29-31 July 1998 Conference Location: Singapore
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)

Treatment: Theoretical (T); Experimental (X)

Abstract: Certain head/slider movements, such as seeking and dynamic load/unload, may lead to head-disk contact/impact. Such head-disk contact/impact is playing more and more important role in the disk drive failure. As a result, new methodology for the in-situ monitoring of the head-disk interaction and the head-disk spacing change caused by such operations is becoming of crucial importance to the disk drive design and manufacturing. By applying a properly selected DC carrier erasure current on the writing head, the spacing variation during such operations can be recorded and tested. The carrier current is selected in such a way that the spacing change will result in a proportional modulation of the head field acting on the media and lead to a proportional modulation of the magnetization difference between adjacent bit cells. The theoretical background of the method, its working principles and major advantages are discussed. The method is of a unique advantage of getting spacing change recorded. The method is also of the advantage of high sensitivity to the variation of head-disk spacing, **comparing** with **other** methods reported with **read / write** head as transducer. (8 Refs)

Subfile: B

Copyright 1999, IEE

27/7/3 (Item 1 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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01530080 E.I. Monthly No: EI8406052773 E.I. Yearly No: EI84031886
Title: MERGED NONVOLATILE RANDOM-ACCESS MEMORY CELL.
Author: Cranford, H. C. Jr.; Hoffman, C. R.
Source: IBM Technical Disclosure Bulletin v 26 n 3B Aug 1983 p 1639-1642
Publication Year: 1983
CODEN: IBMTAA **ISSN:** 0018-8689
Language: ENGLISH
Journal Announcement: 8406
Abstract: A major problem with increasing density of single silicon chip nonvolatile random-access **memories** is that the drive to higher density circuits increases the time required to alter the state of the nonvolatile element when **compared** to acceptable **read / write** times. Secondly, the **number** of store and erase cycles becomes limited. An approach previously taken has been the combining of volatile and nonvolatile cells using both the metal nitride oxide **semiconductor** and floating gate technologies. The present description deals with floating gate technology because of its use of capacitive coupling elements.

File 9:Business & Industry(R) Jul/1994-2005/May 06
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File 16:Gale Group PROMT(R) 1990-2005/May 06
(c) 2005 The Gale Group
File 47:Gale Group Magazine DB(TM) 1959-2005/May 09
(c) 2005 The Gale group
File 148:Gale Group Trade & Industry DB 1976-2005/May 09
(c)2005 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2005/May 09
(c) 2005 The Gale Group
File 570:Gale Group MARS(R) 1984-2005/May 09
(c) 2005 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2005/May 09
(c) 2005 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2005/May 09
(c) 2005 The Gale Group
File 649:Gale Group Newswire ASAP(TM) 2005/Apr 12
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Set	Items	Description
S1	2220852	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	1445599	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS OR CHIP? ? OR MICROCHIP? ?
S3	2209280	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	5214746	TEST OR TESTER? OR TESTED OR TESTING OR TESTS OR SELFTEST? OR BIST OR EVALUAT?
S5	185955	S4(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S6	75528	S4(3N)S1:S2
S7	4028812	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	145582	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	1643559	READ OR READS OR READING
S10	57649	S9(5N) (ANOTHER OR OTHER)
S11	151737	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR THIRD OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWEEN)
S12	15247	S9(5N) (NUMBER OR PAIR?? ?)
S13	601	S7(5N)S8
S14	345	S7(5N)S10
S15	1158	S7(5N)S11:S12
S16	84	S13(S)S14:S15
S17	18	S16(S)S1:S3
S18	12	S16(S) (RAM OR RAMS OR STORAGE OR RAS OR DRAM? ? OR SRAM? ? OR SDRAM? OR RDRAM? OR SLDRAM? OR DDR? ? OR SGRAM? OR DRDRAM? OR DDRAM?)
S19	22	S17:S18
S20	3	S19/2002:2005
S21	19	S19 NOT S20
S22	12	RD (unique items)
S23	62	S16 NOT S19
S24	31	S23/2002:2005
S25	31	S23 NOT S24
S26	22	RD (unique items)

? t22/3,k/6

22/3,K/6 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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10543614 SUPPLIER NUMBER: 53097412 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Tolerant To A Fault.
Alderman, Ray
Electronic Design, 72(1)
Oct 12, 1998
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 938 LINE COUNT: 00079

... two values. This will ensure, to some degree, that the data is valid. When a " write " transaction is done to disk or memory , a " read -and- compare " transaction must follow. This will guarantee that the data was written to memory or disk without errors. In some instances, write transactions are "mirrored." Here, data is written to two different memory locations or two different disk drives. Parity bits and cyclic redundancy check (CRC) are hardware...

File 696:DIALOG Telecom. Newsletters 1995-2005/May 06
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Set	Items	Description
S1	2032359	SEMICOND? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS OR FET OR FETS
S2	1150686	MOSFET? ? OR JFET? ? OR MOS OR CMOS OR IC OR ICS OR CHIP? ? OR MICROCHIP? ?
S3	3259986	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S4	4946934	TEST OR TESTER? OR TESTED OR TESTING OR TESTS OR SELFTEST? OR BIST OR EVALUAT?
S5	105868	S4(3N):(DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S6	40936	S4(3N)S1:S2
S7	4514220	COMPARISON? OR COMPARAT? OR COMPAR??? ?
S8	172839	(READ OR READS OR READING) (10N) (WRITE? OR WROTE OR WRITING OR WRITTEN)
S9	2479280	READ OR READS OR READING
S10	81651	S9(5N) (ANOTHER OR OTHER)
S11	225368	S9(5N) (2 OR 3 OR 2ND OR 3RD OR TWO OR THREE OR SECOND OR THIRD OR PLURALIT? OR SEVERAL OR ADDITIONAL OR ACROSS OR BETWEEN)
S12	19507	S9(5N) (NUMBER OR PAIR?? ?)
S13	598	S7(5N)S8
S14	401	S7(5N)S10

S15 1490 S7(5N)S11:S12
S16 74 S13(S)S14:S15
S17 33 S16/2002:2005
S18 41 S16 NOT S17
S19 37 RD (unique items)

19/3,K/33 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications
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0368436

Readers Serve Up Some Tasty Feedback

Dr. Rebecca Thomas

Unix World, Vol. IX, No. 3, Pg 93

March, 1992

JOURNAL CODE: UNIX

SECTION HEADING: Hands-on Help ISSN: 0739-5922

WORD COUNT: 2,884

TEXT:

...structure. See Listing 3A.

Like the standard UNIX diff command, our cdiff script Listing 3B **reads**
and **compares** two files and **writes** the result to the standard output.
Unlike diff, cdiff shows lines common as well as...

File 347:JAPIO Nov 1976-2005/Jan(Updated 050506)
 (c) 2005 JPO & JAPIO
 File 350:Derwent WPIX 1963-2005/UD,UM &UP=200529
 (c) 2005 Thomson Derwent
 File 348:EUROPEAN PATENTS 1978-2005/May W01
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 File 349:PCT FULLTEXT 1979-2005/UB=20050505,UT=20050428
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 File 324:German Patents Fulltext 1967-200517
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Set	Items	Description
S1	84	AU=TAKEHIGE M?
S2	727	AU=HIBINO S?
S3	23366	AU=YAMADA K?
S4	24168	S1:S3
S5	3214306	SEMICONDUCTOR? ? OR SEMICONDUCTOR? OR SEMI() (COND? ? OR CONDUCT-OR?) OR MEMORY? OR MEMORIES OR FED OR FEDS
S6	1461770	TEST OR TESTER? OR TESTED OR TESTING OR TESTS
S7	1657419	CUT OR CUTS OR MUT OR MUTS OR DUT OR DUTS
S8	35995	S6(3N)S5
S9	171713	S6(3N) (DEVICE? ? OR CIRCUIT? OR CKT? ? OR COMPONENT? OR MODULE? OR UNIT OR UNITS)
S10	1051	S4 AND S7:S9
S11	143104	(COMPARISON? OR COMPARAT? OR COMPAR??? ?) (5N) DATA
S12	2377	S7:S9(20N)S11
S13	2	S4 AND S12

13/9/1 (Item 1 from file: 347)
 DIALOG(R)File 347:JAPIO
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07803074 **Image available**
 SEMICONDUCTOR DEVICE

PUB. NO.: 2003-297100 [JP 2003297100 A]
 PUBLISHED: October 17, 2003 (20031017)
 INVENTOR(s): MIYAZAKI JIYUNRI
 OHARA KUNIHIRO
 HIBINO SUMITAKA
 KONDO AKIYOSHI
 TANIGUCHI KAZUYA
 NARUTOMI HIROSHI
 APPLICANT(s): FUJITSU LTD
 FUJITSU VLSI LTD
 APPL. NO.: 2002-094609 [JP 200294609]
 FILED: March 29, 2002 (20020329)
 INTL CLASS: G11C-029/00; G01R-031/28; G06F-011/22; H01L-021/822;
 H01L-027/04

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device in which a test time for a memory circuit can be shortened.

SOLUTION: In a test of RAM 13, a CPU 12 performs write/read operation of data for the RAM 13. A comparing circuit 15 compares read-data D1 with expected value data D2 whenever the CPU 12 reads read-data D1 from the RAM 13, and stores the compared result in a result register 16. Then, when the CPU 12 finishes read of the read-data 1 for all address, the CPU 12

outputs the comparison result data D3 read from the result register 16 to the outside.

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13/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015250413 **Image available**

WPI Acc No: 2003-311339/200330

XRPX Acc No: N03-247801

Memory circuit testing method e.g. in semiconductor device,
involves selecting memory circuits and comparing read data with one
another and with write data

Patent Assignee: FUJITSU LTD (FUIT); FUJITSU VLSI LTD (FUIV)

Inventor: HIBINO S ; TAKESHIGE M ; YAMADA K

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020188900	A1	20021212	US 200126560	A	20011227	200330 B
KR 2002095028	A	20021220	KR 20022029	A	20020114	200330
JP 2002365338	A	20021218	JP 2001174101	A	20010608	200330

Priority Applications (No Type Date): JP 2001174101 A 20010608

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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US 20020188900	A1		18	G11C-029/00	
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KR 2002095028	A			G11C-029/00	
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JP 2002365338	A		12	G01R-031/28	
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Abstract (Basic): US 20020188900 A1

NOVELTY - Several memory circuits (RAM0-RAM3) are simultaneously selected, and the read/write operation of the memory circuits is performed. The data read from the memory circuits are compared with one another, and one of the read data is also compared with the write data, during the test mode.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) semiconductor device; and
- (2) memory circuit testing system.

USE - For testing random access memory (RAM) circuits in semiconductor device (claimed) such as large scale integrated (LSI) circuit.

ADVANTAGE - Shortens the memory circuit testing time and cost, since the time needed to access the memory circuits becomes shorter by simultaneous selection of the memory circuits.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic block diagram of the semiconductor device.

memory circuits (RAM0-RAM3)

pp; 18 DwgNo 1/15

Title Terms: MEMORY; CIRCUIT; TEST; METHOD; SEMICONDUCTOR; DEVICE; SELECT;

MEMORY; CIRCUIT; COMPARE; READ; DATA; ONE; WRITING; DATA

Derwent Class: S01; T01; U11; U14

International Patent Class (Main): G01R-031/28; G11C-029/00

File Segment: EPI

Manual Codes (EPI/S-X): S01-G02B; T01-J07B1; U11-F01C5; U14-D09



STIC Search Results Feedback Form

CW

EIC 2100

Questions about the scope or the results of the search? Contact **the EIC searcher or contact:**

Anne Hendrickson, EIC 2100 Team Leader
272-3490, RND 4B28

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➤ I am an examiner in Workgroup: Example: 2133

➤ Relevant prior art **found**, search results used as follows:

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art **not found**:

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

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